REMARKS

The present response amends the specification to correct typographical errors. In addition, claims 11 and 12 have been amended. Claims 1-24 remain pending in the captioned case.

Section 112 Rejection

Claims 11-13 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. In response thereto, claims 11 and 12 have been amended in a manner believed to address the concerns expressed in the Office Action. Accordingly, Applicants respectfully request removal of this rejection.

Section 103 Rejection

Claims 1-24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over various combinations of U.S. Patent No. 6,366,989 to Keskar et al. (hereinafter "Keskar"), "General DDR SDRAM Functionality" by Micron Technology (hereinafter "Micron"), U.S. Patent No. 6,955,941 to Bolken (hereinafter "Bolken"), "The Printed Circuit Board Primer" by Eirik Holm (hereinafter "Holm"), and U.S. Patent No. 6,320,758 to Chen (hereinafter "Chen"). To establish a case of *prima facie* obviousness of a claimed invention, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Second, there must be a reasonable expectation of success. As stated in MPEP 2143.01, the fact that references can be hypothetically combined or modified is not sufficient to establish a *prima facie* case of obviousness. *See In re Mills*, 916 F.2d. 680 (Fed. Cir. 1990). Finally, the prior art references must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d. 981 (CCPA 1974); MPEP 2143.03. Specifically, "all words in a claim must be considered when judging the patentability of that claim against the prior art." *In re Wilson* 424 F.2d., 1382 (CCPA 1970). Using these standards, Applicants contend that the cited art fails to teach or suggest all features of the currently pending claims, some distinctive features of which are set forth in more detail below.

Keskar and Micron do not teach or suggest the combination of an execution engine clocked at a first rate and pins for transferring data to and from a memory controller on both the rising and falling edges of a second clock rate, wherein the second clock rate is less than the first clock rate. Present independent claim 1 describes an execution engine and a memory controller. The execution engine is clocked at a first clock rate and the memory controller is clocked at a second clock rate, less than the first clock rate. Pins are adapted to transfer data to and from the memory controller on both the rising and falling edges of the second clock signal transitioning at the second clock rate. Description of the benefits of utilizing a slower clock rate for the memory controller than the execution engine, and applying data transfer on the rising and falling edges is set forth throughout the present specification – particularly when referencing the advantages and disadvantages of SDR and DDR. Unlike SDR, DDR utilizes both true and complementary pairs of clock signals to drive the data signals (DQ) (Specification -- pg. 2, lines 20-31). The distinction between SDR and DDR when applied to SDRAM technology is set forth in Micron. While DDR can enjoy the advantage of higher transfer speed (Specification -- pg. 3, lines 19-27), the higher data transfer rate increases the current loop area and the magnetic flux on the memory controller pins (Specification -- pg. 3, lines 4-17).

Instead of simply applying DDR technology to a memory controller output to increase the data transfer rate, the present claimed invention judiciously decreases the memory controller clocking rate relative to the execution engine. By decreasing the memory controller clocking rate to a second clock rate, the connection of the pins which form the integrated circuit to the printed circuit can be made more cost effective (Specification -- pg. 4, lines 1-16). Instead of requiring flip-chip alignment and solder connection, the present claimed invention can use conductive layers within the printed circuit board connected to the integrated circuit using leads and bonding pads. *See, e.g.,* claims 8, 9, and 13-17. Thus, contrary to the assertions made in the Office Action, it is not merely beneficial to take an SDR teaching and apply DDR transfer for the purpose of increasing data transfer since, as discovered by the present invention, the increased data rate can cause high parasitic inductance and capacitance on the integrated circuit leads (Specification -- pg. 6, lines 4-8). While DDR DRAMs are decreasing in cost and the advantages of higher throughput are apparent, it is not necessarily of benefit to implement DDR memory at twice the data transfer rate as the execution

engine. Thus, "clock throttling is used with the advantages of DDR DRAMs" (Specification -- pg. 6, line 1).

The Examiner agrees that Keskar does not teach data transfer between the memory interface and the memory device occurring on both the rising and falling edges of a second clock (as claimed); however, the Examiner alleges that Micron provides the needed nexus (Office Action -- page 3). The Examiner believes it obvious to one of ordinary skill in the art to combine the SDR teachings of Keskar with the DDR teachings of Micron in order to allow data to be transmitted at a faster rate (Office Action -- pages 3-4). Applicants respectfully disagree. Merely increasing the data transfer rate is not the objective of that which is presently claimed unless, of course, the clocking rate on the memory controller can be throttled downward relative to the execution engine, which is not taught in Micron. Moreover and more importantly, the SDR teachings of Keskar cannot be modified in hindsight to be implemented with DDR technology.

Keskar specifically teaches "the memory interface 66 operates at the speed of the SDRAM memory 40 . . ." (Keskar -- col. 3, lines 57-59). Keskar makes it explicitly clear that the processor clock CK_CLK of the BIU and SDC synchronizes the BIU with the SDC for transfers to and from the SDC (memory controller) from the execution unit (Keskar -- col. 8, lines 66-67). The SDC (or memory controller) receives BIU output data at the leading edge of each clock cycle 212, 214, 216, and 218 (Keskar -- col. 9, lines 6-14; Fig. 6). Thus, data is transferred into the memory controller (SDC) on just the rising edges of a first clock signal sent from the BIU. Converse to a write begin operation shown in Fig. 6 of Keskar, a read end operation is shown in Fig. 7. Again, however, the read operation of SDC is "synchronized to the processor clock ck_clk" (Keskar -- col. 9, lines 46-47). During the rising (positive) edges of each cycle of ck_clk, data is transferred from the SDC to the BIU (Keskar -- col. 9, lines 53-64). Thus, Keskar makes it explicitly clear that all read and write operations between the BIU and the memory controller (SDC) occur only on the rising or positive edges of a clock cycle ck_clk. Moreover, ck_clk is at the first clock rate synchronized to the execution engine. Similar to transfers between the BIU and SDC, Keskar also makes clear that transfers between the SDC and SDRAM occur on leading edges of the memory clock (mclk) (Keskar -- col. 11, line 20 – col. 12, line 21). Thus, data is read from SDRAM or written to SDRAM only during the leading or positive edges of clock cycles of mclk (Keskar -- Figs. 8-9).

Not only does Keskar make clear that the data pins 84 transfer data on only the rising edges of mclk (second clock) or data on pins 70 transfer on only the rising edge of ck_clk (first clock), but nowhere is Keskar is there any mention that data might be transferred in any other fashion. In fact, to modify Keskar to implement DDR rather than SDR would destroy the required operation of Keskar. Not only is there no suggestion to modify, but any proposed modification would change the principle of operation of Keskar. *See* MPEP 2143.01; *In re Ratti*, 270 F.2d 810 (CCPA 1959). Keskar specifically requires that transfers to and from SDC 30 are synchronized with either the execution unit via ck_clk leading edges or mclk of SDRAM leading edges. In fact, the principle of operation of Keskar is to implement a synchronous read and write mechanism, meaning that to effectuate a burst synchronous read/write, then read and write operations must occur on successive leading edges of either ck_clk or mclk.

Therefore, unlike the rationale set forth in the Office Action, Applicants assert that Keskar and Micron cannot be properly combined. In addition, as stated throughout the present specification, there is no advantage in combining Keskar and Micron since the present claims throttle downward the memory controller clock relative to the execution engine. There would be no motivation or expectation of any advantage for downward throttling the memory controller as claimed. The combination of downward throttling of the memory controller with DDR transfer to and from the memory controller is the claimed feature to which the cited references cannot properly address.

Keskar and Micron do not teach the combination of clocking an execution engine with a first clock rate and transferring data between a memory controller and a memory device at both the leading and trailing edges of the second clock. Similar to independent claim 1, independent claim 21 also describes the combination of downward throttling of a memory controller relative to an execution engine and DDR transfers between a memory controller and a memory device. Keskar specifically requires SDR transfers for its burst read and write operations, and Micron provides a disincentive for anyone skilled in the art to downward throttle the clocking rate of a memory controller, and is completely absent of any clocking relativity between a memory controller and an execution engine. Again, the cited references cannot be combined as suggested in the Office Action.

The cited art does not teach or suggest the combination of an execution engine clocked at a first rate and a data bus for transferring data between a memory controller and a memory device at a rate greater than the first clock rate. Independent claim 9 is slightly dissimilar from claims 1 and 21 in that claim 9 describes transferring data at a rate greater than the first clock rate, the first clock rate being that which operates the execution engine. A combination of Keskar, Holm, and Chen were cited against claim 9. Holm and Chen have nothing whatsoever to do with disparity in clock rates or the rate at which data is transferred across a data bus. Keskar notes that data can be burst read from or written to memory via a memory controller; however, the rate of transfer across the data bus linking the memory controller and the memory device is explicitly called out in Keskar to be less than the clock rate applied to execution engine. *See, e.g.,* Keskar description of the SDRAM memory being "typically slower than the processor speed" (Keskar -- col. 3, lines 57-58). Thus, Keskar teaches away from the limitation of claim 9 by requiring the mclk clock and the corresponding synchronous transfer of data to memory being less than (rather than greater than) the first clock rate ck_clk of the execution engine (Keskar -- col. 4, lines 37-38; col. 5, lines 34-37; col. 7, lines 1-3; col. 9, lines 46-47; col. 11, lines 28-30).

In addition to being patentably distinct for at least the same reasons as their respective base claim, several of the dependent claims are also believed separately distinct. For example, cited references lack any teaching of a multiplexer (claim 2) or a multiplexer for sending a second clock upon receiving a power supply (claim 3). Nowhere in the cited references is there any mention of a multiplexer that can select between a first clock and a second clock for clocking a memory controller (claim 6). In addition, claim 6 recites a configuration register and a latch, neither of which are taught by the cited references. As to claim 7, Applicants respectfully disagree that Micron teaches "the memory controller receiving a power supply voltage of 1.25 V" (Office Action, page 4). Instead, Micron indicates that the power supply voltage (V_{DD}) is equal to 2.5 V, and the reference voltage (V_{REF}) is equal to 1.25 V (Micron, page 10).

For at least the foregoing reasons, Applicants believe independent claims 1, 9, and 21, as well as claims dependent therefrom, are patentably distinct over the cited references. Accordingly, Applicants respectfully request removal of this rejection.

CONCLUSION

The present amendment and response is believed to be a complete response to the issues raised in the Office Action mailed January 29, 2007. In view of the remarks herein, Applicants assert that pending claims 1-24 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to LSI Corporation deposit account number 12-2252.

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